



Corres. and Mail
BOX AF

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **HORIGUCHI, Naoto et al.**

Serial No.: 09/726,386

Filed: December 1, 2000

Group Art Unit: 2811

Examiner: Tran, Thien F

P.T.O. Confirmation No.: 1274

AF/2811
#13/B
Andt
ATE
JMcMillan
8/5/03

For: **SEMICONDUCTOR MEMORY WITH FLOATING GATE TYPE FET**

RESPONSE UNDER 37 CFR §1.116
- EXPEDITED RESPONSE -
GROUP ART UNIT 2811

Mailstop After Final
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

July 28, 2003

Sir:

In response to the Office Action dated **April 30, 2003**, please amend the above-identified application as follows:

IN THE CLAIMS:

AMEND claims 1, 3 and 12 and 14 to read as follows:

1. (Amended) A semiconductor memory comprising:
- a semiconductor substrate;
- a tunneling insulating film formed on a partial surface area of said semiconductor substrate,
- said tunneling insulating film having a thinness enough to transmit carriers therethrough by a direct tunneling phenomenon;
- a floating gate electrode formed on said tunneling insulating film;
- a gate insulating film covering a side wall of said floating gate electrode and a partial surface area of said semiconductor substrate on both sides of said floating gate electrode, said gate insulating

RECEIVED
AUG - 1 2003
TECHNOLOGY CENTER 2800

B1